

FPGA Documentation

Lecture 05

Josh Brake

Harvey Mudd College

Outline

- Documentation Overview
- FPGA documentation Bingo
- Manual design mapping exercise
- Quick basic testbench review



















Learning Objectives

By the end of this lecture you should be able to...

- Find basic specs in the FPGA documentation to answer questions about your system like DC logic levels, max clock speed, etc.
- Determine the number of logic cells required by simple Verilog modules.
- Recall how to write a Verilog testbench

Lattice iCE40UP Documentation

Documentation

Quick Reference	Technical Resources	Information Resources	Downloads		
Key Documents Data Sheet Application Note Pin & Package User Manual	Reference Design Product Change Notification Schematic	Product Brochure Quality Assurance White Paper	IBIS Model		
  TITLE ▼	NUMBER	VERSION	DATE	FORMAT	SIZE
<input type="checkbox"/>  iCE40 UltraPlus Family Data Sheet 	FPGA-DS-02008	2.0	9/20/2021	PDF	1.1 MB
<input type="checkbox"/>  Memory Usage Guide for iCE40 Devices 	FPGA-TN-02002	1.7	10/14/2020	PDF	954.3 KB
<input type="checkbox"/>  iCE40 I2C and SPI Hardened IP Usage Guide 	FPGA-TN-02010	1.7	9/11/2020	PDF	1.3 MB
<input type="checkbox"/>  iCE40 SPRAM Usage Guide 	FPGA-TN-02022	1.3	4/16/2021	PDF	912.9 KB
<input type="checkbox"/>  iCE40 Hardware Checklist 	FPGA-TN-02006	2.0	3/10/2022	PDF	355.4 KB
<input type="checkbox"/>  iCE40 Oscillator Usage Guide 	FPGA-TN-02008	1.7	1/25/2021	PDF	675 KB
<input type="checkbox"/>  iCE40 sysCLOCK PLL Design and User Guide 	FPGA-TN-02052	1.4	4/30/2022	PDF	1.3 MB
<input type="checkbox"/>  iCE40 LED Driver User Guide 	FPGA-TN-02021	1.5	11/29/2021	PDF	2 MB

Lattice iCE40UP Documentation

- Info on FPGA chip itself
 - DC logic levels
 - Timing information
 - Package dimensions
 - Pinout information
 - Block diagrams of internal components



iCE40 UltraPlus Family Data Sheet

Data Sheet

FPGA-DS-02008-2.0



Package Diagrams

Data Sheet

FPGA-DS-02053-6.8

UPduino Documentation

Specs specific to the UPduino board

- Schematics
- Supporting hardware
- Programming instructions

UPduino Documentation

tinyVision.ai

UPduino v3.0: PCB Design Files, Designs, Documentation

The UPduino v3.0 is a small, low-cost FPGA board. The board features an on-board FPGA programmer, flash and LED with _all_ FPGA pins brought out to easy to use 0.1" header pins for fast prototyping.

The tinyVision.ai UPduino v3.0 Board Features:

- Lattice UltraPlus ICE40UP5K FPGA with 5.3K LUTs, 1Mb SPRAM, 120Kb DPRAM, 8 Multipliers
- FTDI FT232H USB to SPI Device
- _ALL_ 32 FPGA GPIO on 0.1" headers
- _ALL_ FTDI pins brought to test points
- 4MB SPI Flash
- RGB LED
- On board 3.3V and 1.2V Regulators, can supply 3.3V to your project
- Open source schematic and layout using KiCAD design tools
- Integrated into the open source [APIO toolchain](#)

FPGA Documentation Bingo

Bingo Card

#	Question	Answer	Reference
1	Recommended operating voltage for VCCIO		
2	I/O pin input capacitance		
3	3.3 V LVCMOS Logic Levels		
4	Recommended core input voltage		
5	Maximum speed of sysI/O buffer		
6	Maximum PLL output frequency		
7	Maximum output current		
8	Operating temperature range		
9	Input leakage current		
10	What FPGA device is on the UPduino v3.1 board?		
11	Major elements in a Logic Cell (LC)		
12	What is the range of clock frequencies for the high speed internal oscillator?		
13	How many logic element are on our FPGA?		

Bingo Card

#	Question	Answer	Reference
14	How many EBR memory blocks?		
15	How many SPRAM memory blocks?		
16	What is the difference between EBR and SPRAM?		
17	How many I/O banks?		
18	Data buss skew across a bank of I/Os?		
19	Propagation delay through 4-input LUT?		
20	PIO input register setup time		
21	PIO input register hold time		
22	PIO output register clock to output (Q)		
23	Number of multipliers in the FPGA		
24	Package for our FPGA chip		
25	How many user I/Os does the FPGA chip have?		
26	What is the area of the FPGA package?		
27	What voltage does the FPGA core run on?		

Manual Design Mapping

Going from Verilog HDL to logic cells

- 2-input AND: _____
- 4-input AND: _____
- 5-input AND: _____
- 16-input AND: _____
- Arbitrary function of 5 inputs: _____
- Arbitrary function of 6 inputs: _____

- 2 inverters: _____
- Divide by 3 counter: _____

Wrap up

- FPGA documentation contains important information like logic levels and timing specs
- Learning to navigate the documentation is a skill that must be practiced. Try to browse instead of search.
- As a hardware designer, you should be able to explain how many logic cells