Microprocessor Final Report

Michael Jang and George Wang 12/10/21

Abstract:

A breathalyzer is a device that measures and displays the breath alcohol content (BrAC) of a person. It samples the air that it detects for ethanol, and some models use this to change the voltage output of a printed circuit board (PCB). A simple circuit was constructed to fit the constraints of the analog-digital converter (ADC) on the STM32F401RE microcontroller unit (MCU). The ADC reading is then processed on the MCU and transformed into the appropriate two-digit reading, which is 5 bits long. The MCU then sends this reading over SPI to the MAX10 FPGA on the Arrow MAX1000 PCB. The FPGA then takes this information and time multiplexes rows of LEDs to display the two digits on an 8-by-8 LED matrix. Calibration was done by taking various measurements with a store-bought breathalyzer. This was successfully implemented, and the system as a whole behaves as desired.

Introduction:

The final project of E155 directed students to use the principles taught in the class to design and build a complex system that implements novel hardware not previously used in the labs. A volatile organic compound (VOC) sensor's resistance changes based on the level of a compound it detects in the air around it. Certain ones can detect ethanol, which appears in the breath of a person who has consumed alcohol. Alcohol consumption can have serious consequences, especially when it comes to the operation of motor vehicles, which is why laws are in place based on the blood alcohol (BAC) of a person. Because of this, using a sensor to display the BAC of the user is highly valuable, as it can prevent a person from participating in dangerous activities or getting arrested. This was the motivation behind this project.

The block diagram shown below in Figure 1 shows an overview of the entire breathalyzer system.

Figure 1: Overall System Block Diagram

As seen in the block diagram, the MCU is taking in the input from the VOC sensor and sending converted data to the FPGA, which runs the 8 by 8 LED matrix. The other human input is a button that tells the MCU to take a measurement.

VOC Sensor and Circuit:

The VOC sensor used in this project is the MiCS 5524. This sensor is capable of detecting concentrations of up to 500 ppm of ethanol. The PCB that includes the sensor takes in a 5V and GND input from the MCU, and outputs a voltage that increases with as the concentration of alcohol it detects increases. However, due to reasons that will be explained later, the ADC can only read values between 0V and 3.3V, while the output of the PCB can reach 5V. To combat this, the ADC will read the voltage in between two identical resistors linking the output to ground, which makes the maximum readable voltage 2.5V, which the ADC is able to read.

Figure 2: VOC to MCU Connections

MCU ADC Usage:

The ADC on the MCU converts the analog voltage output of the VOC sensor circuit, which is connected to pin A0 on the MCU, into a 12 bit number, which is the highest resolution possible for this unit. The 12 bit number is output by the ADC according to the Equation 1, with analog voltage on pin A0 as an input:

$$
OUT = IN \cdot ((V_{REF+} - V_{REF-})/2^{N}) \tag{1}
$$

In this case, ${V}_{REF+}$ is 3.3V, ${V}_{REF-}$ is 0V, and N is 12, meaning that the ADC outputs a number from 0 to 4095.

The ADC has the option of aligning the number to the left or the right, and the right-aligned option was chosen because when storing the number in a variable, the code will convert the binary number to a number in decimal format. Right shifting allows this number to be read correctly, rather than being shifted and multiplied by a certain amount.

The ADC has 16 channels to sample the voltages of, and any sequence of channels can be sampled in any order. For this project, the only channel used was ADC_IN0, which connected to pin A0 when it was set as an analog pin. The ADC also has single conversion mode, continuous conversion mode, and scan mode. Single conversion mode was used for this project, as it was desired to take only one measurement at the push of a button, shown in Figure 2. There are also sequence registers that keep track of the amount of channels to sample and what order to do so in. These registers were set to 1 channel and ADC_IN0, respectively.

Transformation to BAC on MCU:

As stated in a previous section, the maximum ethanol concentration that the BAC can detect is 500ppm, which roughly translates to 0.1974% BAC. To represent this fact, the code on the MCU converts the ADC reading to a 5 bit binary unsigned integer between 0 and 19. A calibration curve was found by blowing into a store-bought breathalyzer and then reading the voltage on pin A0 with an oscilloscope. Equation 2 below shows the polynomial curve found to be the calibration curve, where x is the BAC in hundreths of a percentage point.

$$
Voltage = 44.7352 \cdot x^2 - 5527 \cdot x + 207 \, (2)
$$

The code takes into account what ADC outputs these voltages translate to, and properly maps them onto a binary unsigned integer between 0 and 19. This value is then stored onto a variable, which is now ready to be sent to the FPGA via SPI.

MCU SPI Communication:

The MCU communicates the 5-bit value calculated during the prior step to the FPGA. This value is placed into the SPI data register, which is set to 8 bits and most significant bit first, and is shifted out on the rising edge of the SPI clock. The MCU acts as the SPI master while the FPGA acts as the client, except that it does not send data back to the MCU. The clock speed is

set by a prescaler in the RCC and the SPI prescaler. The prescaler of the RCC was 16, and the SPI prescaler was set to 256. This caused the SPI clock to have a frequency of 10253 Hz. This low frequency was chosen so that the FPGA was able to sample the incoming bits while also running slowly enough that digits on the LED matrix did not bleed together. Figure 3 below shows the connections between the FPGA and MCU.

Figure 3: MCU to FPGA SPI Connections

MCU Algorithm:

After initializing and enabling the clock and necessary peripherals, the code enters a while loop and then waits for a button press. Once the button is pressed, pin A1 is driven high which tells the ADC to take a single measurement of the voltage output of the VOC circuit. It stores this measurement in a variable, and then puts that value through the voltage to BAC conversion mentioned in a previous section. A timer on the MCU activates to count to 1 second, which prevents any debouncing issues from causing the ADC to read multiple measurements with one button press. The MCU then sends the 5-bit value over SPI, which ends up being an 8-bit value with 3 leading zeroes. The MCU then waits for the FPGA to respond with a high signal that goes to pin A2, indicating that it has received and implemented the 5-bit number in the way that will be described later in the FPGA section of the report.

FPGA SPI Reception:

The FPGA hardware was programmed to be able to receive the 8-bit serially transmitted data from the MCU by causing it to act as a shift register. Essentially, 8 parallel bits were designated, the 5 least significant of which would be the input to the FPGA LED Multiplexing system that will be described in the next section of the report. Using a flop, at every positive edge of the SCK input from the microcontroller, the value on the H4 pin at that time will be shifted in as the least significant bit. This happens 8 times per transmission, so that the 5-bit number will be used as the input to the multiplexing module. Using a counter, the FPGA's clock runs at 20507 Hertz, twice as fast as SCK. This is to ensure that each of the shifts are detected and that, as mentioned previously, the digits on the LED matrix don't bleed together.

FPGA LED Multiplexing:

The FPGA takes in the 5 least significant bits of the SPI data from the MCU, decodes the data to a percentage (0.00, 0.01, 0.02 . . . 0.20) and displays the data on an LED matrix via multiplexing. A seven state FSM is used to determine which row of the LED is turned on for multiplexing. Combinational logic is used to determine which LEDs to assert based on which row is powered and which number needs to be displayed. Transistors are used to provide power to each row of the LED matrix.

Figure 4: FPGA Block Diagram Without SPI

Results:

The system works as intended. The voltages read on the oscilloscope match the ADC and BAC readings that are read in the debugger in VS Code. The system reacts to the presence of alcohol in many forms. It reacts to the presence of vodka on one's breath, the presence of mouthwash containing alcohol on one's breath, and even the presence of mouthwash on a cotton ball held closely to the sensor. This means that the breathalyzer can be demonstrated in a professional setting while also adhering to COVID regulations, which is what was desired from the system when it was first thought of.

References:

lady ada. Adafruit. <https://learn.adafruit.com/adafruit-mics5524-gas-sensor-breakout> July 2016

[http://www.mecinca.net/ALCOHOLIMETROS_Alcosim/BAC%20BrAC%20conversion%20table\[1](http://www.mecinca.net/ALCOHOLIMETROS_Alcosim/BAC%20BrAC%20conversion%20table[1].pdf) [\].pdf](http://www.mecinca.net/ALCOHOLIMETROS_Alcosim/BAC%20BrAC%20conversion%20table[1].pdf)

https://senseair.com/knowledge/information-and-education/gases/c-h-oh-ethanol/

Bill of Materials:

Appendix A: Breadboard Schematics

FPGA and LED

Appendix B: MCU Code

```
final_project.c
```

```
#include "STM32F401RE GPIO.h"
#include "STM32F401RE FLASH.h"
#include "STM32F401RE RCC.h"
#include "STM32F401RE_ADC.h"
#include "STM32F401RE_SPI.h"
#include "STM32F401RE TIM.h"
#include <string.h> // for strstr()
#include <stdint.h> // for integer types (i.e., uint32_t)
#include <stdio.h> // for sprintf()
uint8 t ADCto5bits(uint16 t adc){
  uint8 t a;
  if (adc > (.207*4096/(3.3*2))) {
    if(adc > (.209*4096/(3.3*2)) }
      if(adc > (.2138*4096/(3.3*2))) {
        if(adc > (.2307*4096/(3.3*2))) {
          if (adc > (.2565*4096/(3.3*2))) {
            if(adc > (.2912*4096/(3.3*2)) ) {
              if(adc > (.3349*4096/(3.3*2))){
                if(adc > (.3875*4096/(3.3*2)) }
                   if(adc > (.4491*4096/(3.3*2))){
                     if(adc > (.5196*4096/(3.3*2)) ) {
                       if(adc > (.5991*4096/(3.3*2)) ){
                         if(adc > (.6875*4096/(3.3*2)))if(adc > (.7849*4096/(3.3*2)) }
                             if(adc > (.8912*4096/(3.3*2)) ) {
                               if(adc > (1.0064*4096/(3.3*2)) ){
                                 if(adc > (1.1306*4096/(3.3*2)) ){
                                   if(adc > (1.2638*4096/(3.3*2)) ) {
                                     if(adc > (1.4059*4096/(3.3*2))}
                                       if(adc > (1.5569*4096/(3.3*2)) ) {
                                         a = 19;else {a = 18;}
                                     }
                                     else {a = 17;}
                                   }
                                   else {a = 16;}
                                 }
                                 else {a = 15;}
                               }
                               else \{a = 14; \}}
                             else {a = 13; }
```

```
}
                          else {a = 12;}
                         }
                         else \{a = 11; \}}
                      else {a = 10;}
                    }
                    else {a = 9; }}
                  else {a = 8;}}
                else {a = 7; }
              }
              else {a = 6; }}
            else {a = 5;}
          }
          else \{a = 4; \}}
        else {a = 3; }}
      else {a = 2; }}
    else \{a = 1; \}}
  else {a = 0; }
  return a;
}
int main(void) {
  // Configure the flash and then set clock to 84 MHz from PLL
 configureFlash();
  configureClock();
  RCC->APB2ENR.ADC1EN = 1;
  // Turn on GPIOA
  RCC->AHB1ENR.GPIOAEN = 1;
  //Enable timer
  RCC->CFGR.HPRE = 0b0001;RCC->APB2ENR.TIM11EN = 1;
  // Set PA0 as an input for the ADC, another pin as input for reading and
another for signaling ready
  pinMode(GPIOA, 0, GPIO_ANALOG);
  pinMode(GPIOA, 1, GPIO_INPUT);
  pinMode(GPIOA, 4, GPIO_INPUT);
```

```
durationTimer();
// Set MISO, MOSI, SCK, and CE
spiInit(0b111, 0, 0);
// Initialize the ADC
ADCinit();
//digitalWrite(GPIOB, 6, 1);
uint16 t b;
//b = measure();uint8 t a;
//a = ADCto5bits(b);//b = measure();//a = ADCto5bits(b);//SPI Stuff
//spiSendReceive(a);
while(1) {
 while(digitalRead(GPIOA, 1) != 1); //wait for button push
 TIMERD->ARR.ARR = (1000 * 2) -1; // Wait for amount of time to pass
  TIMERD->CCR1.CCR1 = (1000 * 2);
  TIMERD->EGR.UG = 1;
 while(TIMERD->SR.CC1IF == 0) {}
 TIMERD->SR.CC1IF = 0;
  durationTimer(); // Reset Timer
 b = measure(); // Measure with ADC
  a = ADCt_05bits(b); //Convert measurement
  //SPI Stuff
 spiSendReceive(a); //Send 5 bit number to FPGA
 while(digitalRead(GPIOA, 4) != 1); // Wait for done signal from FPGA
}
return b+a;
```

```
Date: December 06, 2021 Breathylizer.sv Breathylizer.sv Project: Breathylizer<br>
1 //11/22/2021<br>
2 //George Wang<br>
3 //gewang@g bmc_edu
                                                                                                                      Fage 1 of 7<br>
Page 1 of 7<br>
Page 1 of 7<br>
Revision: Breathylizer
         1 //11/22/2021
         2 //George Wang<br>3 //gewang@g.hm
                    //gewang@g.hmc.edu
         4 //module determining the row we are in<br>5 module Breathylizer
         5 module Breathylizer<br>6 (input logic clk,<br>7 input logic load
          December 06, 2021<br>
1 //11/22/2021<br>
2 //George wang<br>
3 //gewang@g.hmc.edu<br>
4 //module determining the row we are in<br>
5 module Breathylizer<br>
6 (input logic clk,<br>
7 input logic clk,<br>
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9 input logic sck,<br>
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3 //gewang@g.hmc.edu<br>
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2 //george wang<br>
3 //gewang@q.hmc.edu<br>
4 //module determining the row we are in<br>
10 output logic [17:0]<br>
5 module determining the row we are in<br>
10 input logic [17:0]<br>
10 input logic 
       10 input logic sdi, //switches<br>11 output logic [6:0] rowTrans, //transistors<br>12 output logic [7:0] LEDLogic,<br>13 //output logic [7:0] LEDLogic2,<br>14 output logic done);
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7 input logic cla,<br>
7 input logic load,<br>
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4 //gewang@g.hmc.edu<br>
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       28 //transistor logic
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14 //module determining the row we are in<br>
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111 output logic leid) rowTrans, //transistors<br>
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       3<br>
3 module Breathylizer<br>
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3 input logic rest,<br>
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3 input logic for .<br>
110 input logic for .<br>
110 input logic for .<br>
121 output logic [7:0] LEDLogic,<br>
212 
       module Breathylizer<br>
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3 input logic sck.<br>
3 input logic sck.<br>
3 assign row consists.<br>
10<br>
10 input logic sck.<br>
110 input logic sck.<br>
12<br>
212 output logic [5:0] rowTrans, //transistors<br>
13 //output logic (7:0] LEDLogic2,<br>
14 output logic don
       s and the load<br>
1 input logic reader.<br>
11 ionation is reader.<br>
111 ionation is reader.<br>
111 ionation is reader.<br>
112 output logic [7:0] LEDLogic,<br>
13 as output logic (7:0] LEDLogic,<br>
13 as output logic (8:0) row;<br>
15 bout
       34 assign rowTrans [3] = \simrow[5];<br>
10 assign row[100] c = 011.0 percent; //transistors<br>
112 assign row[5] c = [7:0] represent; //transistors<br>
123 //output logic [7:0] LEDLogic2,<br>
143 /output logic (dec)]<br>
16 logic [4:0
       35 assign rowTrans [5] = \frac{1}{2} computed logic [6:0] rowTrans, //transistors<br>111 output logic [6:0] rowTrans, //transistors<br>113 coupled for [6:0] rowTrans,<br>15 coupled for [7:0] LEDLogic2,<br>15 assign rowTrans, spin sets,
       36 
       37 endmodule
       38 
       39 
       40 module LEDFSM<br>41 (input l
       \begin{array}{ll} \textbf{1.61} & \textbf{logic} \textbf{ [4:0]} \textbf{ dataIn};\\ \textbf{1.62} & \textbf{logic} \textbf{ [6:0]} \textbf{ row};\\ \textbf{1.63} & \textbf{logic} \textbf{ [6:0]} \textbf{ row};\\ \textbf{2.7} & \textbf{2.8} & \textbf{CDCbM} \textbf{[UNI} \textbf{ [CMC(R, High);\textbf{[1]}};\\ \textbf{2.8} & \textbf{CDCbM} \textbf{[UNI} \textbf{ [CMC(R, High);\textbf{[1]}};\\ \textbf19<br>
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22 clock-Multi CMO(figh, reset, load, row, done);<br>
22 clock-Multi CMO(figh, reset, load, row, done);
       43 input logic load,
       44 output logic [6:0] row,
       90<br>
201 spi SPI(sck, sdi, dataIn);<br>
21 clockMulti CMO(clk, High);<br>
222 LEDFSM FSMO(High, reset, load, row, done);<br>
223 clockMulti CMO(clip, reset, load, row, done);<br>
223 clockmulti CMO(clip, reset, load, row, done);<br>
223 
       46 
       {1}<br>
27 clockMulti CMO(clk, High);<br>
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275<br>
27 typedef enum logic<br>
//transistor logic<br>
//transistor logic<br>
27 typedef enum logic<br>
27 assign rowTrans[1] = ~row[0];<br>
231 assign rowTrans[1] = ~row[1];<br>
231 assign rowTrans
                   the top LED matrix
       148<br>
148 LEDFSM FSMO(High, reset, load, row, done);<br>
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27<br>
28 assign rowTrans[0] = ~row[0];<br>
28 assign rowTrans[2] = ~row[1];<br>
31<br>
assign rowTrans[2] = ~row[2];<br>
33<br>
38 assign rowTrans[2] = ~row[
       49 
       50 //state register
       51 always_ff @(posedge clk, posedge reset)
       //transistor log(0)<br>
\begin{array}{l} \text{{\tt A}}(r\text{ trans}(\text{real})) = \text{conv}[0] : \end{array}<br>
\begin{array}{l} \text{assign rowTrans}[\text{Q}] = -\text{row}[0] : \end{array}<br>
\begin{array}{l} \text{assign rowTrans}[\text{Q}] = -\text{row}[2] : \end{array}<br>
\begin{array}{l} \text{assign rowTrans}[\text{S}] = -\text{row}[2] : \end{array}<br>
\begin{array}{l} \text{assign rowTrans}[\text{S}] = -\text{row}[6] \ ; \end{array}<br>
\begin\begin{array}{l} \text{{\it X} = 0} \begin{array}{l} \text{{\it X} = 0} \end{array} \begin{array}{l} \text{{\it X} = 0}54 
       54<br>55 //next state logic<br>56 //5 state FSM. 4 r
       56        //5 state FSM. 4 record row information<br>57         always comb
       57 always_comb
       58 case(state)
       39<br>
Assign rowTrans[b] = ~row[b];<br>
assign rowTrans[b] = ~row[b];<br>
39<br>
39 endmodule<br>
(imput logic clk,<br>
(imput logic load,<br>
input logic load,<br>
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output logic load,<br>
output logic load,<br>
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       Sassign rowirans[b] = ~row[b];<br>
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       endmodule<br>
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141 (input logic clk,<br>
input logic clat,<br>
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All (input logic CIk,<br>
42 input logic CIk,<br>
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42 input logic Cik,<br>
44 output logic (6:0) row,<br>
44 output logic (6:0) row,<br>
44 output logic (6:0) row,<br>
46 output logic (4:0) {R0, R1, R2, R3, R4, R5, R
       Module LEDESM<br>
44 else next logic clk,<br>
(input logic load,<br>
143 input logic load,<br>
44 else news logic (6:0) row,<br>
45 else output logic (6:0) row,<br>
46 extertype state, next<br>
46 extertype state, nextstate;<br>
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43 input logic clk.<br>
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46 output logic [6:0] row,<br>
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1 input logic clk.<br>
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16 input logic clks<br>
output logic (Ecd) row.<br>
46 experimenting in the class of the column of the column<br>
47 typedef enum logic (4:0) (RO, R1, R2, R3, R4, R5, R6,R7,R8} statetype; //we wont u<br>
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       1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1991 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992 | 1992
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surpur logic load<br>
else next<br>
de typedef enum logic (4:0) (RO, R1, R2, R3, R4, R5, R6,R7,R8} statetype; //we wont u<br>
the top LED matrix<br>
de statetype state, nextState;<br>
\frac{1}{2} always. Ff @(nosedge clk, posedge rese
       44<br>
output logic Le:01 row,<br>
the comparison logic (4:01 fRO, R1, R2, R3, R4, R5, R6,R7,R8} statetype; //we wont use<br>
the comparison, and the comparison<br>
49<br>
149 State register<br>
always free distance comparison<br>
\frac{1}{2} al
       (1991 comp):<br>
The top LED matrix comp):<br>
The top LED matrix compute (4:0) {RO, R1, R2, R3, R4, R5, R6,R7,R8} statetype; //we wont u<br>
46<br>
46 estate register<br>
201 //state register<br>
201 //state register<br>
201 //state register<br>
       47<br>
The top date from logic [4:0] (RO, R1, R2, R3, R4, R5, R6,R7,R8} statetype; //we wont use<br>
148 statetype state, nextState;<br>
49 statetype state, nextState;<br>
161 always_comb<br>
171 always_comb<br>
171 always_comb<br>
171 always_
       4<br>
The top LED matrix of the U.S. Next, R.S., R4, R.S., R6, R/, R6} state<br>
The top LED matrix else nextstate;<br>
always_fr@(posedge clk, posedge reset)<br>
52<br>
22 if (reset) state <= R0;<br>
else state <= mextstate;<br>
else state <=
       the boundary<br>
148 State register<br>
//state register<br>
21 always ff @Cnosedge clk, posedge reset)<br>
21 always ff @Cnosedge clk, posedge reset)<br>
251 always five class tase c= R0;<br>
77: State FSM-4 frecord row information<br>
77: S
       951 /state register, nextstate;<br>
149<br>
147 always ff @fopsedge clk, posedge reset)<br>
17 always ff @fopsedge clk, posedge reset)<br>
17 always combined in the capital state <= nextstate;<br>
152<br>
152<br>
162<br>
162<br>
162<br>
162<br>
162<br>
162<br>
       %<br>
201 //state register<br>
always rf @Copsedge clk, posedge reset)<br>
151 always can be can be can be can be can be called the<br>
253 //next state logic<br>
275 state SM. 4 record row information<br>
278 always comb<br>
28: if (load) nex
```


378


```
Date: December 06, 2021 Breathylizer.sv Project: Breathylizer 
  451<br>452 default: LEDLogic = 8'b11111111;
  te: December 06, 2021<br>
451<br>
452 default: LEDLogic = 8'b11111111;<br>
453 endcase<br>
454 endmodule<br>
455<br>
455<br>
456<br>
456<br>
457<br>
458 //9/8/21
  453 endcase
  454 endmodule
  455 
  456 
  457 
  458 
  459 //9/8/21
  460 //George Wang
  461 //gewang@g.hmc.edu
  462 //module for generating clock signal at around 2.4Hz
  463 //Referenced Better Verilog Counter Idiom
  464 module clockMulti
  te:December 06,2021 Breathylizer.sv<br>
451 default: LEDLogic = 8'b11111111;<br>
453 endcase<br>
454<br>
455 endmodule<br>
455 endmodule<br>
455 //9/8/21<br>
456 //George Wang<br>
460 //George Wang<br>
461 //gewang@q.hmc.edu<br>
461 //gewang@q.hmc.edu<br>
  te:December 06, 2021<br>
451<br>
451<br>
452 default: LEDLogic = 8'b11111111;<br>
454<br>
453 endmodule<br>
465<br>
455<br>
456 //9/8/21<br>
460 //George Wang<br>
460 //George Wang<br>
460 //George Wang<br>
462 //module for generating clock signal at around 
  467 
  468 logic [15-1:0] LEDHigh;
  469 
  470 always_ff @(posedge clk)
  471 LEDHigh <= LEDHigh + 56;
  Breathylizer.sv<br>
472<br>
4212 default: LEDLogic = 8'b11111111;<br>
4623<br>
4628<br>
4628<br>
4648<br>
4648 endmodule<br>
467<br>
467<br>
467<br>
467<br>
467 /gevang@g.hmc.edu<br>
461 /gevang@g.hmc.edu<br>
467 /medule for generating clock signal at around 2.4Hz
  473 
  472<br>473<br>474 endmodule<br>475
  475 
  476 
  477 module spi(input logic sck,
  478<br>463<br>463<br>463 endocate it:EbDogic s billilili;<br>463<br>468 //9/8/21<br>468 //George Wang<br>460 //George Wang<br>464 //George Wang<br>464 //George Wang<br>462 //Module for generating clock signal at around 2.4Hz<br>462 //Module for generating
  479<br>4644<br>4644 endmodule<br>4656 / MacMarang Clock signal at around 2.4Hz<br>467 / George wang<br>461 / George wang<br>461 / Generation Section (The Conter Idom<br>463 / Medie and Better Verilog Counter Idom<br>468 / Medie (Chrowlition);<br>466
  480 
  4916<br>4918 //9/8/21<br>461 //George @g.hmc.edu<br>461 //George @g.hmc.edu<br>461 //geodalenced @etter verilog Counter Idiom<br>463 //module ClockMultie verilog Counter Idiom<br>465 //module ClockMultie verilog Counter Idiom<br>465 //input lo
  482 always_ff @(posedge sck)
  483<br>488 //9/8/21<br>460 //georgie Parms.edu<br>462 //georgie Parms.edu<br>462 //module roof generatives verilog Counter Idiom<br>463 //module roof generatives verilog Counter Idiom<br>465 (original club in the club of the couple of the 
  484 
  448 //Sevarge wang<br>460 //George wang<br>462 //module for generating clock signal at around 2.4Hz<br>462 //mediate for generating clock signal at around 2.4Hz<br>464 (input logic clk,<br>climate inclusion of the class of the constraint
  486 
  487 
  488 endmodule
  489
```